In the Claims:

1-19. (canceled)

20. (previously presented)An electronic system comprising:

A. a functional circuit having a mode input lead receiving a mode signal to place the functional circuit in one of a functional mode in which the functional circuit operates normally and a test mode in which at least part of the functional circuit is disabled; and

B. a selector circuit having a mode output lead connected to the mode input lead of the functional circuit and having a pair of clock leads separate from the functional circuit, only one of the clock leads at one time receiving a clock signal that controls the state of the mode signal formed on the mode output lead.

21. (previously presented)The system of claim 20 in which the test mode is a by-pass mode.

22. (previously presented)The system of claim 20 in which the selector circuit state machine circuits coupled to the pair of clock leads.

23. (previously presented)The system of claim 20 in which the pair of clock leads are both capable of receiving and sending clock signals.

24. (previously presented)The system of claim 20 in which the selector circuit includes a state machine circuit, and each of

the clock leads is coupled to the state machine circuit through a clock input buffer and is connected to the other clock lead through a clock output buffer.

25. (previously presented)The system of claim 20 in which the selector circuit includes another pair of clock leads separate from the functional circuit and at least one of the four clock leads receives a clock signal that controls the mode signal.

26. (previously presented)The system of claim 20 in which the selector circuit includes another pair of clock leads separate from the functional circuit, and each of the another pair of clock leads is coupled to the state machine circuit through a clock input buffer and is connected to the other clock lead through a clock output buffer.

27-34. (canceled)